Overview

SolidPC is a bus protocol verifier based on formal verification technology. It reads the RTL description of a design block, and checks its compliance with the AMBA protocol family from ARM. Compliance can be checked for AHB-full, AHB-lite, APB, and AXI. SolidPC supports Verilog, VHDL, plus mixed-language descriptions, and runs automatically.

SolidPC Solution

Averant has teamed-up with ARM to develop SolidPC, a static property-checking tool that addresses the issue of protocol compliance. SolidPC implements a formal and exhaustive proof of correctness using properties (rules) to describe specific aspects of the AMBA protocol.

The complete rule set will fully verify a design against the required AMBA protocol. Rules that pass exhaustively demonstrate there are no input or reachable state conditions that could cause the design to fail that part of the protocol - something extremely difficult to prove with simulation.

The entire protocol rule set has been thoroughly verified by ARM and Averant, and is embedded within the SolidPC product to provide a quick and easy, push-button tool.

The tool uses a rules-based approach to design verification. If a rule fails, the system creates a testbench with vectors for simulation. If a rule does not pass exhaustively the system creates a simulation monitor - a model that can be used in simulation to highlight violations of a rule.
Simple Flow

SolidPC guides the user through the steps to setup the compliance test:

Map Signals
Signals in the design are mapped to names defined in the AMBA standard.

Select Rules
The user selects which rules are to be applied to the design under test. Many interfaces implement only a sub-set of the protocol (e.g., no locked transfers). If a rule is de-selected, then a converse rule is automatically enabled (e.g., the device must never attempt locked transfers.)

Run Verification
Each protocol rule is submitted to the formal engine for proving against the design under test. SolidPC explores every possible legal combination of inputs to see if a rule holds true in all cases. If it does, the rule is passed exhaustively.

Clear Results

There are three possible outcomes for each rule applied to the design.

1. The rule passes exhaustively:
The design passes for all possible legal input values.

2. The rule fails:
Failing rules are listed with an explanation of why they failed, and a reference in the AMBA specification where the rule is defined. SolidPC also produces a Verilog or VHDL testbench with stimulus to demonstrate the protocol failure within a simulation environment.

3. The rule is partially proven:
The rule holds for a given number of cycles after reset, but a full proof was not achieved. SolidPC will produce a simulation monitor for further analysis of the rule within a simulation environment.

Solid Benefits

Verify your designs for AMBA compliance in a rigorous and efficient manner. Reduce risk and meet time-to-market pressures. Produce solid designs quickly and with confidence.

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