Sequential Equivalency Checker

Product Features

◆ Handles multi-million gate designs
◆ Supports Verilog, VHDL and mixed descriptions

◆ Exhaustive analysis

◆ Advanced match finding

◆ Error trace generation
◆ Compatible with standard power reduction flows

◆ Integrates with 3rd party debug tools

Overview

SolidSEC verifies that two versions of a circuit are functionally equivalent after sequential optimizations are performed on one circuit. Examples of such optimizations are clock gating and retiming which occur during power reduction optimizations.

SolidSEC was built on Averant's formal verification technology but many custom engines were added to improve performance and capacity.

Verification closure for the power reduction flow

With the growing importance of reducing the power consumption of SoCs, increasingly aggressive power optimization techniques are being introduced in design flows, including sequential ones.

Traditional verification techniques such as simulation and combinational equivalency checking cannot conclusively demonstrate that those modifications did not introduce functionality changes.

SolidSEC provides a way to guarantee that the intended functionality is preserved in the power-optimized circuit, providing closure to the overall power reduction flow.
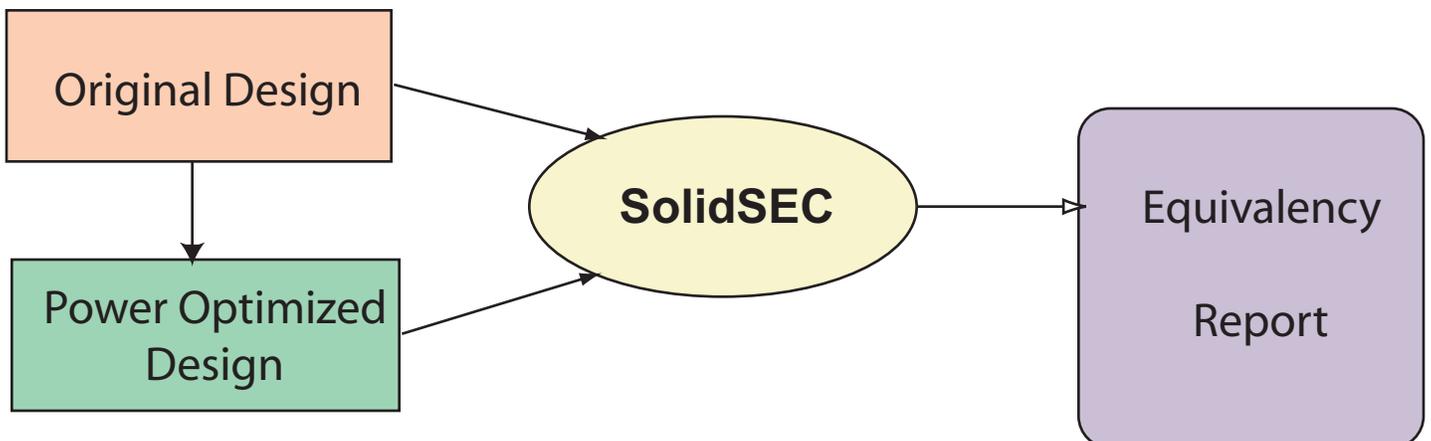
Proprietary technology

Averant has been working on the technology needed to successfully implement sequential equivalency checking for a number of years, and in collaboration with customers, industrial and educational partners. Included in SolidSEC are unique proprietary algorithms which combined with Averant's state of the art formal engines provide a powerful equivalency tool which can easily be included in any design flow.

Also available is a fast combinational equivalency checker (CEC) to solve simple matching problems and reserve the more advanced techniques for the hard problems.

Versatile Solution

SolidSEC can be used to verify either manual design modifications or those introduced automatically by 3rd party solutions. All of the standard design representations such as Verilog, VHDL and mixed designs are supported.

When equivalency fails, traces demonstrating the discrepancy are generated in commonly used formats such as VCD and testbenches. Automatic export to some 3rd party solutions is also available, facilitating debug operations.

Solid Benefits

SolidSEC provides a powerful solution to the crucial verification step of power reduction flows. It is an indispensable tool to keep up with current design challenges when getting functionality right and keeping power consumption low are vital to obtain a competitive edge.