AVERANT ANNOUNCES SOLIDTC:
TIMING CONSTRAINTS VERIFIER

Alameda, Calif. – January 24, 2005 – Averant Inc., a leading provider of advanced verification technology for RTL designs, today announces the availability of SolidTC, a fully automatic verifier for timing exceptions, based on Averant's formal verification tool Solidify and augmented with new algorithms designed for this task.

False and multicycle paths are a subset of timing constraints known as timing exceptions. They are used to exclude those paths the user believes cannot be responsible for delay from consideration during static timing analysis. To ensure the manufactured chip will work at speed, all timing exceptions must be correct. Currently, manual inspection or gate level simulations are used for this purpose. This process is time-consuming and error-prone especially in cases where the exception paths are complex.

SolidTC is a fast and high capacity (multi-million gate) tool that can guarantee the correctness of timing exceptions. The inputs to the tool are the design in Verilog, VHDL or mixed formats, and the timing constraints in SDC (Synopsys Design Constraints) format, both of which are part of a normal design process. The tool then specifies which constraints are incorrect, and for those generates a vector which sensitizes the exception path.

"Ensuring the correctness of timing constraints improves quality, reduces manual effort, and reduces risk" said Averant's President, Ramin Hojati. "We were the first company to recognize that property verification will become mainstream, and provided the design community with production level tools for the task. We are again pleased to be a leader in offering timing exception verification technology in production ready quality to the design community."

"Constraint verification, especially the correctness of timing exception, is one area of concern to any design manager," said Nagendra Cherukupalli, senior director of technology at Cypress Semiconductor, Corp.. "We are monitoring the developments in this area with great interest and are looking forward to including such tools into our design flow."

Availability and Pricing
SolidTC is available immediately, and may be requested at info@averant.com.

About Averant
Averant Inc., founded in 1997, is a privately held EDA firm pioneering new methodology and technologies for static formal verification. Averant provides Solidify™ a robust formal verification engine that provides the basis for property-based design verification, protocol verification, timing constraint verification, and automatic design checks – all without the need for simulators or test vectors. These tools are easily adopted into the design flow, and help improve quality, reduce risk, and speed the design process. For more information, see our Web site at http://www.averant.com.