averant

SolidTC™

Timing Constraint Verifier

Product Features

- Handles multi-million gate designs
- Supports Verilog, VHDL, and mixed descriptions
- Push-button operation
- Exhaustive analysis
- Effort-level capability controls run-time
- Error trace generation
- Requires only design and SDC files
- No impact to current design flow

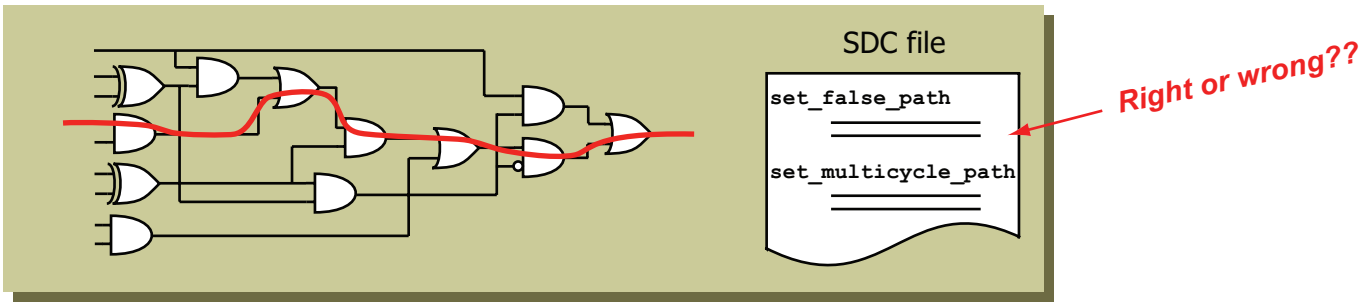
Overview

Timing closure is one of the 3 most critical problems faced by design teams today. Debugging incorrect timing constraints add weeks, even months to project schedules. SolidTC is a timing constraint verification tool based on formal verification technology. It verifies false path and multi-cycle path (MCP) constraints quickly and exhaustively. SolidTC supports Verilog, VHDL and mixed design descriptions. It takes as input an SDC file and outputs a pass/fail for each constraint. SolidTC integrates seamlessly with all modern design flows.

Critical Impact

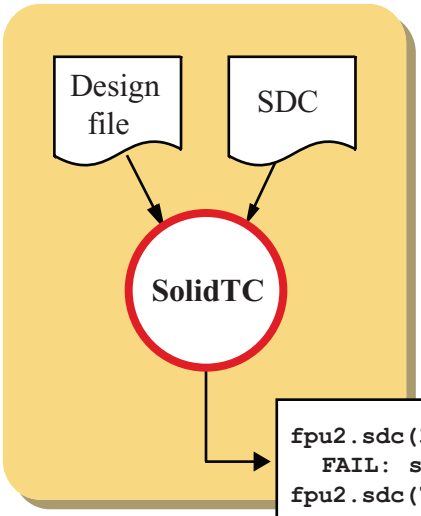
Current designs have thousands of false paths and MCP constraints. Whether generated manually or automatically, incorrect timing constraints can leave chips with critical timing bugs that can cause recalls, re-spins, and redesigns, each costing hundreds of thousands of dollars. Worse still, delays in getting to market and missed opportunities can be devastating.

Checking false and multi-cycle paths is currently done by visual inspection, which is time consuming and error prone. A rigorous and automated way of verifying such constraints would be an enormous improvement to this process.



Powerful Solution

SolidTC from Averant is a powerful and practical solution for verifying timing constraints. It improves productivity and accuracy by a thorough algorithmic examination of your constraints, as opposed to simple manual inspection. SolidTC also generates simulation vectors for incorrect timing constraints, avoiding the need to create them by hand. The thorough verification provided by SolidTC allows you to use a methodology that relies on automatically generated constraints, by ensuring those constraints are correct.



Simple Flow

Once your RTL description is complete, you can develop your timing constraints manually or synthesize them automatically. Simply check your constraints by submitting your design and SDC file to SolidTC for verification.

```
fpu2.sdc(3):
  FAIL: set_false_path -from {in1[*]} -through {sig1[*]} -to {out1[*]}
fpu2.sdc(75):
  FAIL: set_multicycle_path 2 -from {in2[*]} -through {sig2[*]} -to {out2[*]}
```

Advanced Technology

SolidTC includes new timing constraint verification algorithms designed to be thorough and efficient. It's built upon the formal verification engine of Solidify™, a technology that's been used for over 5 years on the most advanced and complex designs.

Solid Benefits

SolidTC accelerates timing closure by verifying the correctness of false path and MCP timing constraints, enabling you to reduce project risks and meet time-to-market pressures.

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