Averant Announces A Significant Update to Solidify

Averant releases Solidify 3.0, introducing significant performance improvements, support for OVA and PSL, improved Auto Checks, Verilog 2001 and System Verilog support, and improved debugging

Solidify™ 3.0 includes
· Significant performance optimizations allowing some properties to run orders of magnitude faster.
· Support for PSL as an input language, with support for PSL output forthcoming.
· Support for OVA as both an input language and as an output from HPL
· Support for mixed Verilog-VHDL designs, some Verilog 2001 and SystemVerilog constructs
· New HPL constructs such as X, Z, labels, and additional temporal sequencing operators
· Significant improvements to Auto Checks such as extensive support for X-assignment propagation, error reporting database with merge capability, and numerous other improvements
· New debugging environment offering new features and increased performance with test bench generation capabilities

Alameda, CA, May 14, 2004 – Averant Inc., the leader in static functional verification software for RTL level Verilog and VHDL designs, today announced the release of Solidify 3.0.

Solidify is an easy to use high performance static functional verifier. Release 3.0 introduces a new proof engine capable of running some properties orders of magnitude faster than prior versions, resulting in increased productivity and extending the applicability range of property verification. The traditional engine has also been enhanced to run faster on most properties. Additionally, some properties on designs including multiple clock domains and some properties involving arithmetic operations run orders of magnitude faster. The engines are complimentary with each being strong in a different problem domain.

Assertions, also known as properties, describe behavior a design should always exhibit or never exhibit. By writing a complete set of properties, the full functionality of a design unit may be checked. Assertions may be run in simulators and also formally proven with Solidify. *If a property passes in Solidify, there is no legal set of input vectors for which the design can fail.*

In Assertion-Based Verification paradigm, properties are the center of the verification activities. Averant was one of the first companies promoting this methodology. To better support assertion-based verification, Solidify processes assertions in a variety of language formats. In version 3.0, Solidify supports two new property languages supported by leading simulators, namely OVA and PSL. Additionally, as HPL continues to be a mature, easy to use, and well-supported property language, converters from HPL to OVA and PSL are provided. This allows Solidify users to use the language best suited for their needs, and reuse that intellectual property in virtually any environment. In the future, Averant plans to support other property languages such as SVA.

Solidify's native language, HPL, continues to be widely used for property verification. It also serves as a common platform to which other languages are compiled. In Solidify 3.0, HPL has been enhanced by providing labels and associated routines for manipulating them, support for X and Z values in the property language, additional temporal sequencing operators, better support for continuous assignments, and improved support for open-ended properties.

Solidify 3.0 supports mixed Verilog and VHDL designs. Additionally, popular constructs from Verilog 2001 and SystemVerilog are supported.

Automatic checks continue to be an important application of property verification. Solidify 3.0 significantly improves ease-of-use of the automatic checks by providing an XML-based error database with merge and summary reporting capability, very refined dead code analysis capable of pinpointing X-propagation problems and poorly specified FSM's, improved error reporting, quality and performance improvements.

A good debugging environment improves productivity. In release 3.0, the debugging environment is rewritten in C for improved performance. In addition to being able to write VCD, text and HTML outputs, the users can now write test benches, which can be run in existing simulation-based debugging environments.

The enhancements in release 3.0, including the ones mentioned above and others, have been driven by customer requests arising from the use of Solidify on customer designs.

“Solidify has been effectively used in numerous customer designs, facilitating faster functional closure, improving the quality of designs, and increasing productivity”, says Ramin Hojati, president of Averant. “Release 3.0 contains many of the improvements our users have been asking for. This release represents a significant milestone in the property verification field”.

Availability and Pricing

Solidify 3.0 will be available on CD-ROM or FTP in June 2004, and may be requested by email at info@averant.com. Solidify 3.0 will be sent to all Solidify customers that subscribe to maintenance. Solidify is available for PC's running Windows NT4.0/2000/XP or Linux Red Hat 7.2 or later, and for workstations running Sun Solaris 2.6/2.7/2.8.

Solidify, which includes Verilog input, VHDL input, property verification in HPL, converters from HPL to other property languages, and auto checks, is priced at $40,000. The coverage option is priced at $8,000. Mixed Verilog-VHDL support and each additional property language are options priced at $15,000 each. All pricing is for one floating perpetual license with maintenance being 20% of the list price in the US market.

About Averant

Averant, Inc., founded in 1997, is a privately held EDA company pioneering the new methodology and technologies for static functional verification. Averant provides Solidify™, a design tool that delivers unprecedented performance in block-level verification for RTL designs. It is a high-capacity, static RTL analysis tool that verifies the functional behavior of Verilog or VHDL blocks without using simulators or test vectors. Solidify improves design quality, reduces risk and uncertainty, shortens design cycles, and reduces the need for simulation based verification. Averant’s products are easily incorporated into synthesis, IP reuse, and FPGA design flows. Averant is on the web at www.averant.com, or can reached by email at info@averant.com